A One Turn Delay Feedback with a fixed frequency clock. Application to the CERN SPS synchrotron.

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WHO AM I… AND MY THESIS…

Javier Galindo; PhD candidate at Universitat Politècnica de Catalunya (Barcelona, Spain)
Last years; at CERN. Wolfgang Höfle, Philippe Baudrenghien.

DIGITAL ARCHITECTURES FOR BEAM SYNCHRONOUS PROCESSING

Processing tunes its response to the frequency variations of the signal during the energy ramp

Problem source (synchrotrons);

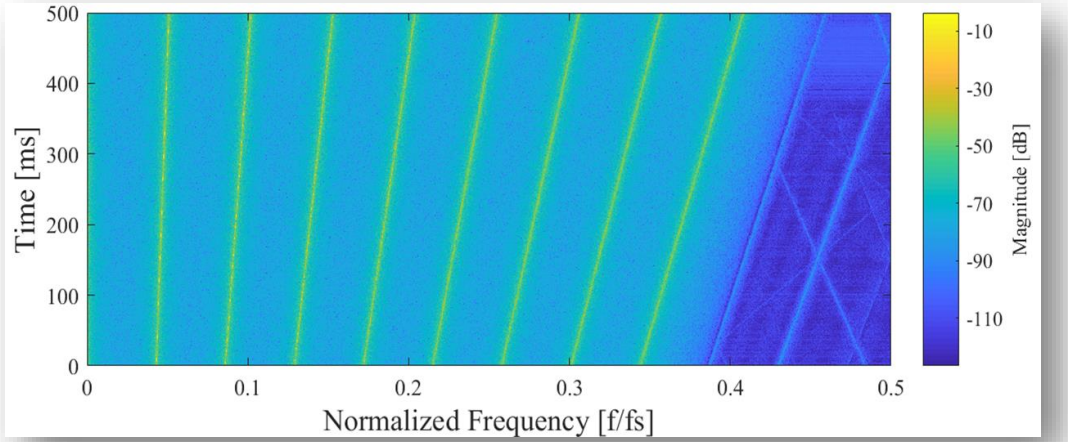
Beam Revolution Frequency harmonics:

- e^- ; *fixed RF, no LLRF tuning*
- *hadrons; swept RF, tune the LLRF*

Used in many applications\algorithms

Beam Loading Compensation

Bunch by Bunch Feedbacks

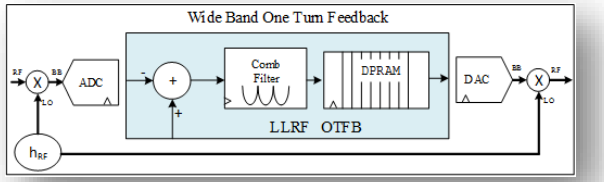


Gentle linear RF ramp

BSP IN TRANSIENT BEAM LOADING COMP.

Big machines; One Turn Feedbacks (OTFB)

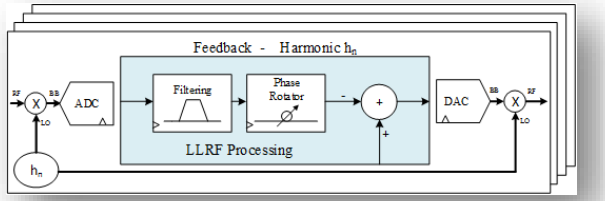
(many harmonics in the regulation BW)



Swept clock does the tuning;
Comb filter (+ 1 Turn delay)

Small machines; Multi-harmonic RF feedback

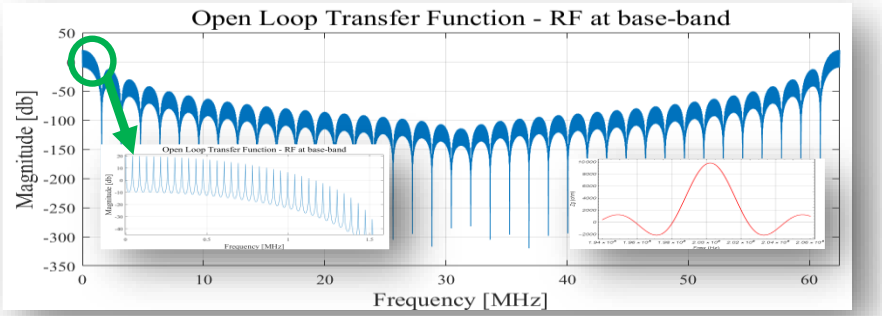
(few harmonics in the regulation BW)



Mixer LO does the tuning;
f_{rev} to base band

CERN SPS 200 MHz case:

Circumference of nearly 7 Km
Revolution Frequency 43 KHz
Regulation BW +/- 5 MHz
(approx. 116 f_{rev} single side)



OTFB comb filter

$$H_{comb}(z) = \frac{1-a}{1-a\,z^{-N}}$$

Define N to match T_{rev} at f_s

$$T_{rev} = N \cdot T_s$$

The Swept Clock f_s does the job with the ramp

The *discrete representation* of the f_{rev} harmonics is tuned to the *discrete comb filter* Ω_{comb} by the *swept* f_s clock

$$\Omega_{comb} = 2\pi \frac{f_{rev}\,(1+\Delta)}{f_s\,(1+\Delta)} = \frac{1}{N} : \text{constant}$$

STATIC HARDWARE

BOUSSARD 1983

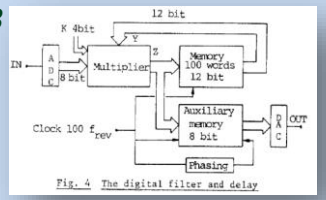
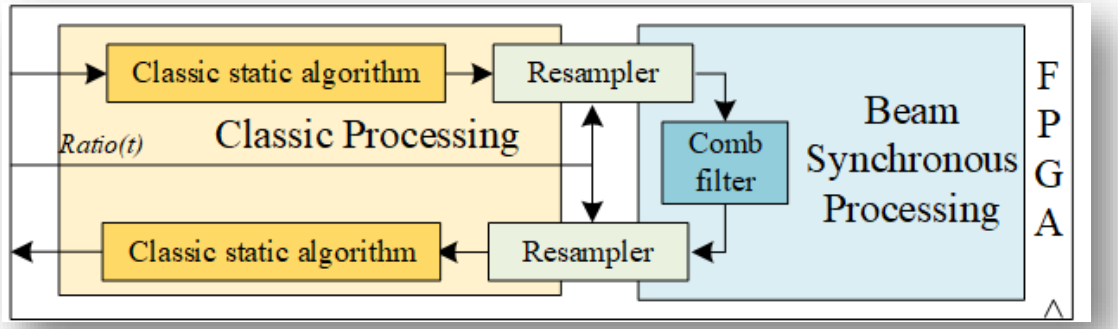


Fig. 4 The digital filter and delay

MOVING TO FIXED FREQUENCY CLOCK

RESAMPLING: “modern” alternative to swept clock



BSP region between two resamplers;

-*Variable sampling rate*

-*Static processing hardware*

-Input resampler; ***Tunes*** *signal to processing*

-Output resampler; ***Recovers original*** *sampling rate*

Inverse resampling ratio

FPGA Implementation of the BSP region:

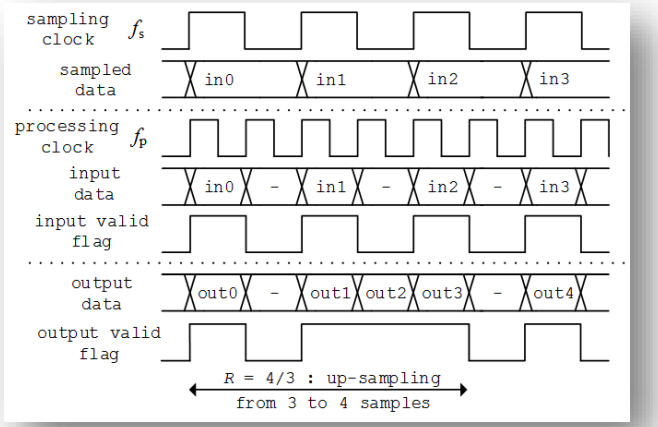
- Clocking:

  Sampling f_s and ***Processing*** f_p clocks need **not** to be equal

  -*Abstract sampling from processing*

  -*Decouple data-path “clocks”*

$$f_p = M \cdot f_s$$



- Resampler:

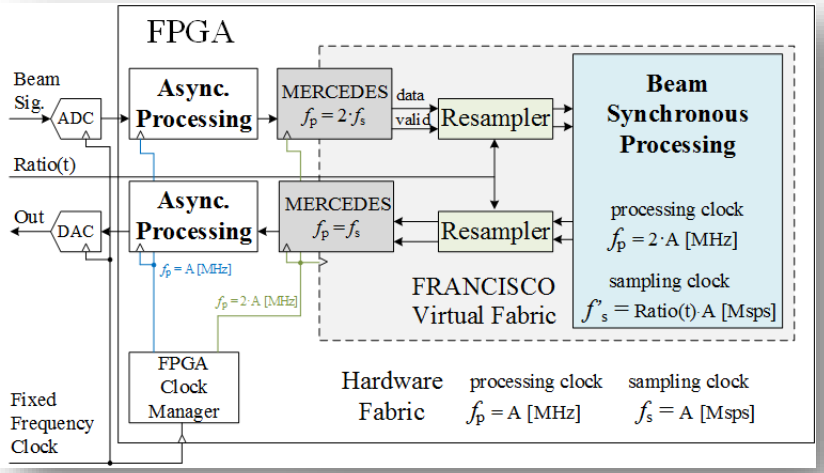
-*Fixed processing clock*

-*Decoupled data-path*

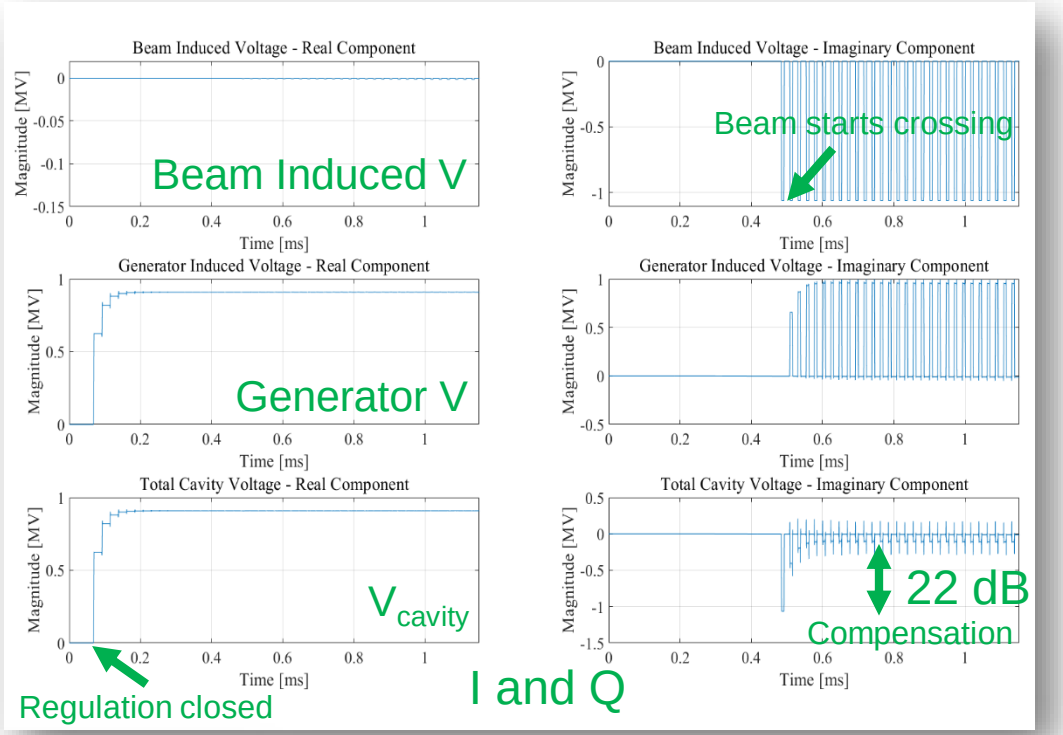
-*Arbitrary and Real Time Variable Resampling Ratio*

SOME RESULTS

BSP hardware architecture

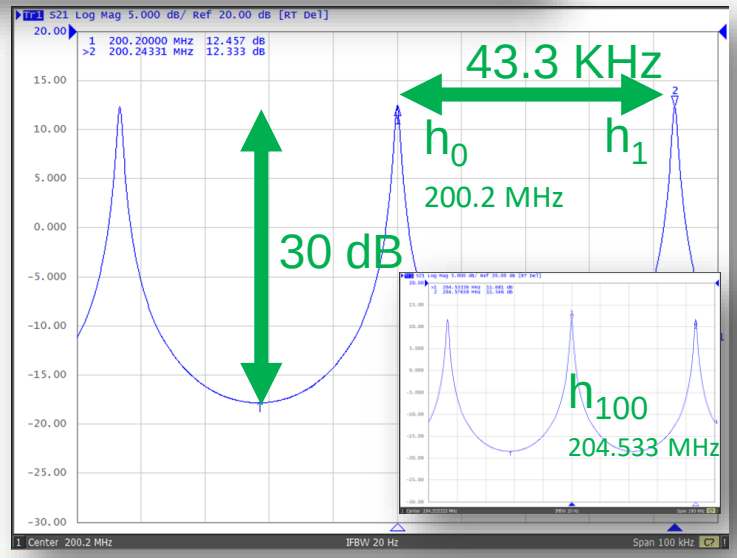


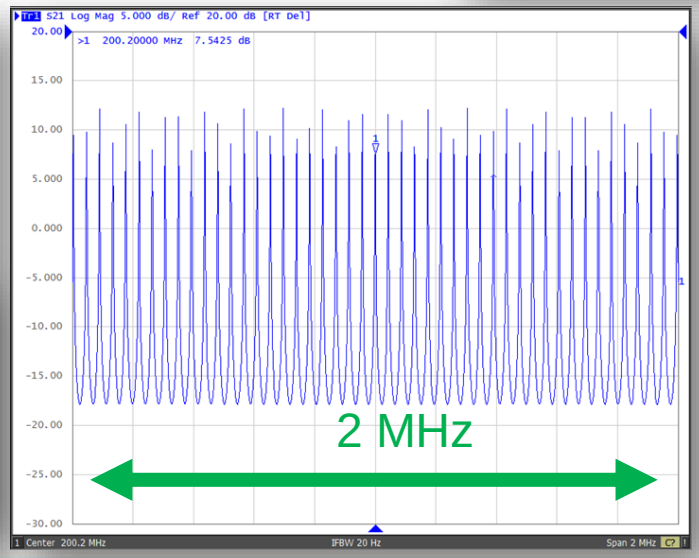
Simulations: OTFB *Transient Beam Loading*

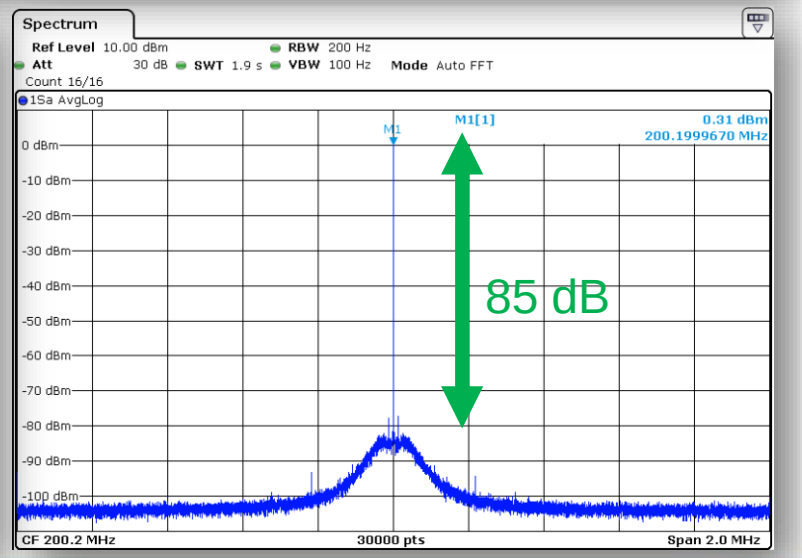


Hardware: *Resampling and BSP*

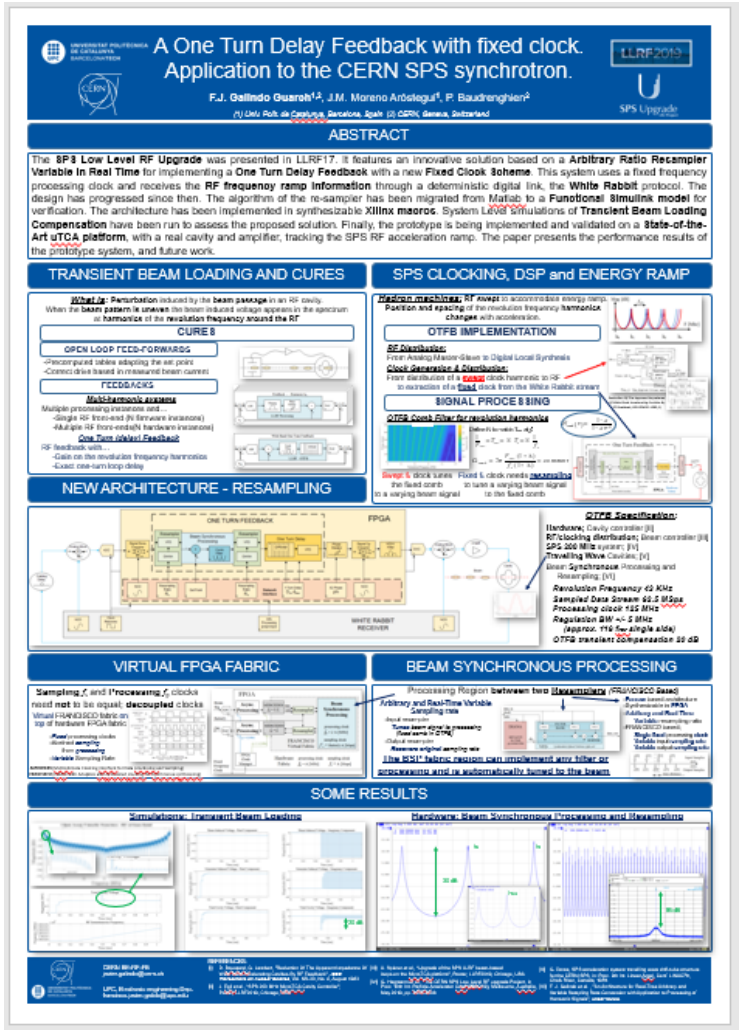
RF @
200.2 MHz
H4620 :
43.3 KHz
Fixed Point:
S0.16
Comb:
a = 15 / 16
G = 10







THANK YOU



You have seen the solution for the OTFB but the architecture can host any other BSP algorithm

Other uses of the BSP and resampler…

A. Spierer et al., “Upgrade of the SPS LLRF beam-based loops on the MicroTCA platform”, Poster, LLRF2019, Chicago, USA

J. Egli et al., “SPS 200 MHz MicroTCA Cavity Controller”, Poster, LLRF2019, Chicago, USA